IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] This application is a continuation of U.S. Patent Application Serial No. 10/150,902, filed May 17, 2002, pending, which application is related to U.S. Patent Application Serial No. ~~09/944,465~~ 09/944,465, filed August 30, 2001 and entitled MICROELECTRONIC DEVICES AND METHODS OF MANUFACTURE, and to the following U.S. Patent Applications filed on even date herewith: Serial No. 10/150,893, entitled INTERPOSER CONFIGURED TO REDUCE THE PROFILES OF SEMICONDUCTOR DEVICE ASSEMBLIES AND PACKAGES INCLUDING THE SAME AND METHODS; Serial No. 10/150,892, entitled METHOD AND APPARATUS FOR FLIP-CHIP PACKAGING PROVIDING TESTING CAPABILITY; Serial No. 10/150,516, entitled SEMICONDUCTOR DIE PACKAGES WITH RECESSED INTERCONNECTING STRUCTURES AND METHODS FOR ASSEMBLING THE SAME; Serial No. 10/150,653, entitled FLIP CHIP PACKAGING USING RECESSED INTERPOSER TERMINALS; and Serial No. 10/150,901, entitled METHODS FOR ASSEMBLY AND PACKAGING OF FLIP CHIP CONFIGURED DICE WITH INTERPOSER.

Please replace paragraph number **[0005]** with the following rewritten paragraph:

[0005] Wire bonding and TAB attachment techniques generally begin with attaching a semiconductor die by its back side to the surface of a carrier substrate with an appropriate adhesive, such as an epoxy or silver solder. In wire bonding, a plurality of fine wires is discretely attached to bond pads on the semiconductor die and then extended and bonded to corresponding terminal pads on the carrier substrate. A dielectric ~~encapsulant~~ encapsulant, such as a silicone or ~~epoxy~~ epoxy, may then be applied to protect the fine wires and bond sites. In TAB, ends of metal traces carried on a flexible insulating ~~tape~~ tape, such as a ~~polyimide~~ polyimide, are attached, as by thermocompression bonding, directly to the bond pads on the semiconductor die and corresponding terminal pads on the carrier substrate.

Please replace paragraph number **[0010]** with the following rewritten paragraph:

[0010] For example, United States Patent ~~5,710,071~~ No. 5,710,071 to Beddingfield et al. discloses a fairly typical flip chip attachment of a semiconductor die to a substrate and a method of underfilling a gap between the semiconductor die and substrate. In particular, the semiconductor die is attached face down to the substrate, wherein conductive bumps on the die are directly bonded to bond pads on the upper surface of the substrate, which provides the gap between the die and substrate. The underfill material flows through the gap between the semiconductor die and the substrate via capillary action toward an aperture in the substrate, thereby expelling air in the gap through the aperture in the substrate in an effort to minimize voids in the underfill material. However, such an underfilling method still is unnecessarily time consuming due to having to underfill the entire semiconductor die. Further, the flip chip attachment technique disclosed in United States Patent ~~5,710,071~~ No. 5,710,071 exhibits difficulties in aligning the conductive bumps with the bond pads on the substrate and requires the expense of having a third metal reroute in the substrate.

Please replace paragraph number **[0016]** with the following rewritten paragraph:

[0016] The conductive bumps may be bonded to the conductive terminals at the bottoms of the recesses by reflowing the bumps, curing the bumps, ultrasonic bonding of the bumps to the terminals, thermal compression bonding of the bumps to the terminals, or by other techniques known in the art, depending upon the bump material selected. Further, a conductive paste or other nonsolid conductive material may be provided on the bumps or within the recesses prior to disposing the bumps in the recesses. Alternatively, bumps in the form of solder balls may be disposed in the recesses prior to alignment of the semiconductor die with the interposer substrate, or higher melting point metal or alloy bumps may be provided in a conductive paste in the recesses or on the bumps, after which the die may be aligned with the interposer substrate and attached thereto. In addition to enhancing electrical connection reliability between the conductive bumps and the interposer terminals, a nonsolid conductive material may be used to compensate for any noncoplanarity between the semiconductor die and interposer substrate due

to varied bump sizes, recess depths and planarity variation in the opposing, adjacent surfaces of the semiconductor die and interposer substrate. As noted, an adhesive element on the surface of the interposer substrate facing the semiconductor die may be used in some embodiments as a height controller and may also help compensate for any irregularities in the coplanarity between the semiconductor die and the interposer substrate.

Please replace paragraph number **[0017]** with the following rewritten paragraph:

[0017] The semiconductor device assembly of the present invention may also be configured with one or more openings extending through the interposer substrate at a location or locations from the surface facing or facing away from the semiconductor die to provide communication between the one or more openings to each of the multiple recesses in the interposer substrate. This configuration facilitates dispensing of dielectric filler material through the opening or openings into the recesses and around the bumps. The opening or openings may be substantially coincident with the configuration of recesses and comprise gaps between conductive pad or terminal portions of conductive traces extending across the recesses or may comprise slots ~~over~~ over, or laterally offset ~~from~~ from, the recesses and in communication therewith and, if offset, a side of each recess being open to the slot. In the first and second instances, dielectric filler material may be introduced directly into the recesses through the gaps between the sides of the conductive trace extending over each recess and the periphery of the recess wall adjacent the trace. In the latter instance, dielectric filler material may be introduced into the slots to travel laterally therefrom into the recesses. Further, if a vertical standoff is employed between the interposer substrate and the semiconductor die, dielectric filler material may be introduced through a slot or other opening through the interposer substrate in the center region thereof and caused to flow therefrom into the recesses through the mouths thereof, even if not in communication with the opening, and to the periphery of the semiconductor die (if desired) through the standoff. A solder mask applied to the side of the interposer substrate facing away from the semiconductor die for forming solder bumps on the conductive elements of the interposer substrate, as noted below, may also be employed as a dam to prevent flow of underfill

material through openings extending through the dielectric layer of the interposer substrate. This aspect of the present invention substantially enhances underfill integrity while decreasing process time.

Please replace paragraph number **[0018]** with the following rewritten paragraph:

[0018] The flip chip semiconductor device assembly of the present invention may also include solder balls or other discrete external conductive elements attached to the terminals or conductive traces extending from the terminals over the surface of the interposer substrate facing away from the semiconductor die. The discrete external conductive elements are employed to interconnect the semiconductor device assembly with higher-level ~~packaging~~ packaging, such as a carrier substrate, for example, in the form of a printed circuit board. The semiconductor die of the flip chip semiconductor device assembly may be fully or partially encapsulated by a dielectric encapsulation material or may be left exposed.

Please replace paragraph number **[0022]** with the following rewritten paragraph:

[0022] The interposer substrate may be fabricated from a flexible material including a flexible dielectric member, a conductive member, an adhesive on the flexible dielectric member and a solder mask over the conductive member. The flexible dielectric member may comprise a polyimide layer which overlies the solder mask with the conductive member therebetween. The conductive member comprises a pattern of conductive traces formed by etching of a conductive layer carried by the flexible dielectric member or by printing traces on the flexible dielectric member using conductive ink. Trace ends may be enlarged at the intended locations of the recesses to define pads for the ~~terminals~~ terminals, and the traces may extend therefrom to enlarged bump pads sized and placed for formation of external conductive elements thereon for connection to higher-level packaging. The recesses may be formed through the flexible dielectric member from the surface thereof opposite the conductive member by etching, mechanical drilling or ~~punching~~ punching, or laser ablation, wherein each of the recesses extends to a terminal of a conductive trace and is sized and configured to receive a conductive bump of the

semiconductor die. The flexible dielectric member may also optionally include another patterned conductive layer thereon over the surface of the flexible dielectric member to face the semiconductor die. The interposer substrate of the present invention may also be formed of other interposer substrate materials such as a BT resin, FR4 laminate, FR5 laminate and ceramics.

Please replace paragraph number **[0049]** with the following rewritten paragraph:

[0049] FIG. 23 illustrates encapsulating a semiconductor die in a flip chip-type assembly and the flip ~~chip~~ chip-type semiconductor assembly attached to another substrate via solder balls, according to the present invention;

Please replace paragraph number **[0069]** with the following rewritten paragraph:

[0069] Conductive bumps 156 preferably comprise, but are not limited to, conductive balls, pillars or columns. The material of conductive bumps 156 may include, but is not limited to, any known suitable metals or alloys thereof, such as lead, tin, copper, silver or gold. Conductive or conductor-filled polymers may also be employed, although gold and PbSn solder bumps are currently preferred. The conductive bumps 156 may be of uniform characteristics ~~there~~ therethroughout or include, for example, a core of a first material (including a nonconductive material) having one or more conductive layers of other materials thereon. Conductive bumps 156 are preferably formed on the active surface 152 of each semiconductor die 150 at a wafer level, but such is not required. Conductive bumps 156 may be formed by metal evaporation, electroplating, stencil printing, gold stud bumping by wire bonders, or any suitable method known in the art.

Please replace paragraph number **[0070]** with the following rewritten paragraph:

[0070] FIG. 6B depicts interposer substrate 110 mounted to semiconductor die 150 to form flip chip semiconductor device assembly 160, wherein such assembly 160 provides that each of the conductive bumps 156 is substantially inserted in a corresponding recess 120 of interposer substrate 110 and engages with the conductive pad or terminal 122 at the bottom of

each of the recesses 120. Such semiconductor device assembly 160 may be initially attached by the adhesive element 116 carried on the first surface 112 of the interposer substrate 110. The conductive bumps 156 on the semiconductor die 150 may then be bonded to the conductive pads or terminals 122 in the recesses 120 of interposer substrate 110 by, for example, reflowing the conductive bumps 156 (in the case of solder bumps) or curing the conductive bumps 156 (in the case of conductive or conductor-filled polymer bumps) as known in the art. Other methods of bonding known in the art may be utilized, such as ultrasonic or thermal compression.

Please replace paragraph number **[0076]** with the following rewritten paragraph:

[0076] FIGS. 9A - 9B depict simplified cross-sectional views of a variant of the above-described third method comprising a fourth method of preparing, mounting and bonding interposer substrate 110 to a semiconductor die 150 in a flip chip semiconductor device assembly 160. Such variant is similar to the third method as described in FIGS. 8A - 8D of providing conductive paste in each of the recesses 120, except the conductive bumps 156 are initially unattached to the bond pads 158 of the semiconductor die 150. As depicted in FIG. 9A, the conductive bumps 156 in the form of balls, such as metal balls, are embedded into the conductive paste 182, which was previously spread into the recesses 120 of the interposer substrate 110. The bond pads 158 in the semiconductor die 150 are aligned with the conductive bumps 156 in the recesses 120 in the interposer substrate 110 and then mounted thereto, as depicted in FIGS. 9A - 9B. The conductive paste 182 may comprise a solder wettable to both bond pads 158 and conductive pads or terminals 122 or a conductive or conductor-filled adhesive. It will also be understood and appreciated that conductive bumps 156 may themselves comprise solder, such as a PbSn solder, and conductive paste 182 ~~eliminated~~ eliminated, or also comprising a compatible solder.

Please replace paragraph number **[0079]** with the following rewritten paragraph:

[0079] As shown in FIG. 10, a dielectric filler material 166 (commonly termed an "underfill" material) may be optionally applied through opening 130. The method employed to

apply the dielectric filler material 166 ~~is preferably by~~ preferably involves dispensing under pressure from dispenser head 164, but may include any method known in the art, such as gravity and vacuum injecting. In this manner, the dielectric filler material 166 may be applied into the opening 130, move as a flow front through the multiple segments 132 and into each of the recesses 120 to fill a space around the conductive bumps 156, bond pads 158 and conductive pads or terminals 122. The dielectric filler material 166 may be self-curing through a chemical reaction, or a cure accelerated by heat, ultraviolet light or other radiation, or other suitable means may be used in order to form at least a semisolid mass in the recesses 120. Such dielectric filler material 166 provides enhanced securement of the components of flip chip semiconductor device assembly 160 as well as precluding shorting between conductive elements and protecting the conductive elements from environmental concerns, such as moisture. As such, compared to the conventional underfilling of the entire semiconductor die, the semiconductor device assembly 160 of the present invention requires less time since the filler material may only be directed to fill the recesses 120 or, rather, any leftover space within the recesses 120 proximate the interconnections, *i.e.*, conductive bumps 156.

Please replace paragraph number **[0081]** with the following rewritten paragraph:

[0081] FIG. 10 also depicts conductive balls 162, such as solder balls or any suitable conductive material, provided at the conductive pads 126 exposed at the second surface 114 of the interposer substrate 110. Such conductive balls 162 may be provided prior or subsequent to dispensing the dielectric filler material 166, and formation thereof, if formed of solder, is facilitated by solder mask 118 (see FIG. 2) and apertures therethrough placed over locations of conductive pads 126. Of course, conductive balls 162 may comprise other materials, such as conductive epoxies or conductor-filled epoxies, and may comprise other shapes, such as bumps, columns and pillars. Once the conductive balls 162 are formed on or attached to the interposer substrate 110 and the dielectric filler material 166 has been provided (if desired or necessitated), the semiconductor die 150 may then be either partially or fully encapsulated by an encapsulation apparatus 178 with a dielectric encapsulation material 168 as depicted in FIG. 11. In the case of

partially encapsulating the semiconductor die 150, encapsulation material 168 may be dispensed by dispenser head 164 about the periphery of the semiconductor die 150 so that the back side or surface 154 of the die is left exposed. In the case of fully encapsulating the semiconductor die 150, encapsulation material 168 may be provided by dispensing, spin-coating, glob-topping, pot molding, transfer molding, or any suitable method known in the art. It is currently preferred that such encapsulation material 168 be applied to the back side or surface 154 of the semiconductor die 150 (which may include applying at the wafer level, as by spin-coating) prior to dispensing additional encapsulation material 168 about the periphery of the semiconductor die 150 in order to facilitate fully encapsulating the semiconductor die 150.

Please replace paragraph number **[0083]** with the following rewritten paragraph:

[0083] FIG. 12 depicts a flip chip semiconductor device assembly 160 including a heat transfer element 180. The heat transfer element 180 may be provided over the first surface 112 of the interposer substrate 110 and under the adhesive element 116 (not shown) as a thin, thermally conductive material. The heat transfer element 180 may also be provided on the active surface 152 of the semiconductor die 150 to abut the first surface 112 of the interposer substrate 110. Another option is to provide the heat transfer element 180 on the back side or surface 154 of the semiconductor die 150 as shown in broken lines. Such heat transfer element 180 is configured and located to thermally conduct heat generated from the electrical components of the semiconductor die 150 and to remove such heat from the flip chip semiconductor device assembly 160 and to reduce the incidence of thermal fatigue in the interconnections and circuitry of the semiconductor device assembly 160 and, specifically, the semiconductor die 150 as well as to reduce operating temperatures.

Please replace paragraph number **[0090]** with the following rewritten paragraph:

[0090] FIG. 18 depicts a top plan view of a third embodiment of an interposer substrate 710 having a center recess configuration. The interposer substrate 710 of the third embodiment is similar to the first embodiment, except the interposer substrate 710 of the third

embodiment does not include openings extending to recesses 720 at a second surface 714 of interposer substrate 710. First surface 712 carries one or more adhesive elements 716 thereon. Second surface 714 carries a plurality of conductive elements in the form of conductive pads or terminals 722 and conductive traces 724 which may have associated therewith conductive pads 726 for formation of discrete conductive elements thereon for connecting interposer substrate 710 to external circuitry. Solder mask 718 (FIG. 19) may be employed to dam the bottoms of recesses 720 as well as the bottom of channel 740. Alternatively, channel 740 may be of lesser depth than recesses 720 and not extend all the way through dielectric layer 711. FIGS. ~~18-20~~ 18 - 20 depict a channel 740 formed in a first surface 712 of interposer substrate 710, wherein FIGS. 19 and 20 depict cross-sectional views of interposer substrate 710 taken along respective section lines 19 and 20 in FIG. 18. The channel 740 may, but is not limited to, extend to a depth substantially the same as the recesses 720 and is configured to extend longitudinally alongside the row of recesses 720 so that each recess 720 may directly communicate with the channel 740. A portion of the interposer substrate 710 between each recess 720 comprises alignment fingers 742, which are defined by forming the recesses 720 and the channel 740 therealong in interposer substrate 710. Such alignment fingers 742 provide an alignment characteristic so that the conductive bumps may be positioned and aligned with the conductive pads or terminals 722 when being disposed in the recesses 720.

Please replace paragraph number **[0092]** with the following rewritten paragraph:

[0092] FIG. 22 depicts the channel 740 having a channel opening 744 at a side periphery of the semiconductor assembly 760, through which dielectric filler material 166 may be introduced. Such filler ~~material~~ material 166 may be dispensed from dispenser head 164 proximate the channel opening 744, wherein dielectric filler material 166 may flow and fill in spaces around the conductive bumps 756 in the recesses 720. Such process may be employed with the semiconductor assembly 760 horizontal, vertical, or at any angle which may promote the filler material to fill the recesses 720. The dielectric filler material 166 introduction may also be enhanced by a vacuum or suction means to optimize the time it takes to fill in the recesses 720.

Further, if conductive pads or terminals 722 cover the bottoms of recesses 720, each conductive pad or terminal may be provided with a hole therethrough through which air may be expelled by the flow front **F** of dielectric filler material 166 or to which a vacuum may be applied. As in the previous embodiments, semiconductor die 750 may be fully encapsulated, including back side 754, with encapsulation apparatus 178 and dispenser head 164 or partially encapsulated with dispenser head 164, as depicted in FIG. 23.

Please replace paragraph number **[0095]** with the following rewritten paragraph:

[0095] The interposer substrate 210 includes a first surface 212 and a second surface 214 with multiple recesses 220 formed in the first surface 212 and openings 230 having passages (not shown) formed in the second surface 214. The recesses 220 formed in the interposer substrate 210 are made to correspond in substantially a mirror image with the bump configuration on each of the semiconductor dice 251 of the semiconductor wafer 250. In this manner, the interposer substrate 210 may be attached to the semiconductor wafer 250 via an adhesive element 216 on the first surface 212 of the interposer substrate 210 so that the conductive bumps 256 on the semiconductor wafer 250 are inserted into and substantially received within the multiple recesses 220 formed in the interposer substrate 210 to form a wafer scale assembly 260, as depicted in FIG. 24B. The wafer scale assembly 260 may then be singulated or "diced" along the borders 253 of the semiconductor wafer 250 via a dicing member such as a wafer saw 280 to form individual, singulated flip chip semiconductor device assemblies that each include one or more semiconductor dice 251 having the separated interposer substrate 210 of the present invention mounted thereon.

Please replace paragraph number **[0096]** with the following rewritten paragraph:

[0096] Also at the wafer level and as previously described in association with FIGS. ~~6A-6B~~ 6A - 6B, ~~7A-7B~~ 7A - 7B, ~~8A-8D~~ 8A - 8D, ~~9A-9B~~ 9A - 9B, the conductive bumps 256 may be bonded to the conductive pads or terminals in the recesses 220 to, therefore, mechanically bond and electrically connect the semiconductor wafer 250 to the wafer scale

interposer substrate 210. In addition, dielectric filler material may be applied through the openings 230 and conductive balls 262 may be provided on the bond posts on the second surface 214 of the interposer substrate 210, either prior to dicing the wafer scale assembly ~~260~~ 260, or subsequent thereto.

Please replace paragraph number **[0099]** with the following rewritten paragraph:

[0099] FIG. 27 depicts a cross-sectional view of a semiconductor assembly 460 including a semiconductor die 450 mounted face down to an interposer substrate 410 having a peripheral recess configuration and an alternative method of applying dielectric filler material 166 to the semiconductor assembly 460. In particular, dielectric filler material 166 may be applied by dispenser head 164 around the periphery of the semiconductor die 450 so that the dielectric filler material 166 flows under the semiconductor die 450 and around the conductive bumps 456 adjacent the die periphery. As such, the dielectric filler material 166 is only needed proximate the conductive bumps 456 and not under the entire die as done conventionally. The semiconductor die 450 may be left exposed or encapsulated by encapsulation apparatus 178, which may provide encapsulation material 168 to the semiconductor assembly 460 via dispensing, spin-coating, glob-topping, ~~depositing~~ depositing, ~~or transfer~~ transfer molding, or any other suitable method known in the art. It is preferred that such encapsulation material 168 be applied to the back surface 454 of the semiconductor die 450 at the wafer level or prior to dispensing the dielectric filler material 166 about the periphery to facilitate fully encapsulating the semiconductor die 450.

Please replace paragraph number **[0100]** with the following rewritten paragraph:

[0100] Further, in this alternative embodiment, it is preferred that the semiconductor die 450 is assembled and bonded to the interposer substrate 410 with the conductive bumps 456 disposed in the conductive paste 182 as described in FIGS. ~~8A-8D~~ 8A - 8D and ~~9A-9B~~ 9A - 9B; however, this alternative may also employ the methods described in FIGS. ~~6A-6B~~ 6A - 6B

and ~~7A-7B~~ 7A - 7B for assembling and bonding the semiconductor die 450 to the interposer substrate 410.

Please replace paragraph number **[0102]** with the following rewritten paragraph:

[0102] As a further approach to implementing the present ~~invention~~ invention, and as depicted in FIG. 29, an interposer substrate 110 may be provided having conductive traces 124 laminated thereto, the bottoms thereof being fully covered or, optionally, uncovered by solder mask 118, and a conductive bump 156a formed by reflow (if solder) or curing (if an epoxy) of a mass of conductive paste 182 at the bottom of each recess 120. A dielectric filler material 166 ~~in~~ is then disposed over conductive bumps 156a in each recess 120 as shown. A semiconductor die 150 carrying a like plurality of conductive bumps 156b arranged for superimposed contact with conductive bumps 156a when semiconductor die 150 is aligned with interposer substrate 110 is then aligned over interposer substrate 110 and vertically pressed thereagainst as depicted by arrow M, the die placement motion squeezing the nondielectric filler material laterally outward so that conductive bumps 156a and 156b meet and make conductive contact. Adhesive elements 116 may, as shown, be used, or may be omitted, as desired.

Please replace paragraph number **[0103]** with the following rewritten paragraph:

[0103] In a variation of the approach of FIG. 29, it is also contemplated that, in lieu of using dielectric filler material 166 and to provide an interposer substrate-to-die adhesive instead of using a separate adhesive element 116, a nonconductive film ~~NCF~~ NCF, as shown in broken lines in FIG. 29 ~~be~~ may be disposed over interposer substrate 110 after formation of conductive bumps 156a thereon and prior to assembly with a semiconductor die 150 carrying conductive bumps 156b. When the semiconductor die 150 and interposer substrate 110 are pressed together, conductive bumps 156a and 156b will penetrate the nonconductive film to initiate mutual electrical contact therebetween. Suitable nonconductive films include the UF511 and UF527 films offered by Hitachi Chemical, Semiconductor Material Division, Japan.

Please replace paragraph number **[0105]** with the following rewritten paragraph:

[0105] The present invention may employ a recess lateral dimension or diameter which is far in excess of the lateral dimension or diameter of an associated conductive bump, thus greatly facilitating bump and recess alignment by loosening required dimensional tolerances. For example, a ~~75μm~~ 75 μm bump may be employed with a 120 μm recess using a 175 μm pitch.

Please replace paragraph number **[0107]** with the following rewritten paragraph:

[0107] In addition, the use of a flexible interposer substrate easily accommodates minor variations between heights of various conductive bumps and lack of absolute planarity of the semiconductor die active surface as well as that of the terminals. Further, encapsulation, if desired, of some or all portions of the periphery and back surface of the semiconductor die by a variety of methods is greatly facilitated, as is incorporation of a thermally conductive heat transfer element such as a heat sink without adding complexity to the package. If an adhesive element employing a tape is used to secure the semiconductor die and interposer substrate together, different bond pad arrangements are easily accommodated without the use of a liquid or gel adhesive and attendant complexity of disposition. Further, tape may be used to resolve a lack of coplanarity of the conductive bumps on a semiconductor die or at the wafer level and to provide cushioning during die attach to the interposer substrate, as sufficient force may be applied ~~sufficient~~ to ensure contact of the conductive bumps with terminals without damage to the assembly. More specifically, during semiconductor die placement, the tape may act as a stopper or barrier and as a cushion. If a conductive paste is deposited in a via, the tape acts as a barrier to prevent paste contamination of the surface of the semiconductor die. If, on the other hand, solidified conductive bumps are used, when heat is used to soften the bump material, the tape acts as a stopper as well as a cushion when the bump material relaxes. In addition, tape accommodates the "spring back" effect exhibited when force used to assemble a semiconductor die and interposer substrate is released, helping to keep the interconnection or joint together. These advantages are applicable to both rigid or flexible interposer substrates.

Please replace paragraph number **[0109]** with the following rewritten paragraph:

[0109] While the present invention has been disclosed in terms of certain preferred embodiments and alternatives thereof, those of ordinary skill in the art will recognize and appreciate that the invention is not so limited. Additions, deletions and modifications to the disclosed embodiments may be effected without departing from the scope of the invention as claimed herein. Similarly, features from one embodiment may be combined with those of another while remaining within the scope of the invention. For example, the opening 130 and segments 132 described in association with the centrally aligned recess configuration in interposer substrate 110 in FIGS. ~~1-3~~ 1 - 3, may also be provided and adapted to the I-shaped recess configuration of interposer substrate 310 and the periphery recess configuration of interposer substrate 410 in FIGS. 25 and 26, respectively. In addition, the present invention is contemplated as affording advantages to assemblies using rigid as well as flexible interposer substrates, although, of course, some features and embodiments may offer greater utility to flexible interposer substrates.